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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,263	11/19/2001	Michael A. Lamson	TI-31189	8850

7590

02/28/2003

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EXAMINER

MALDONADO, JULIO J

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 02/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.



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Office Action Summary

Application No.

09/989,263

Applicant(s)

LAMSON ET AL.

Examiner

Julio J. Maldonado

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2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 November 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 and 18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 and 18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 November 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. The non-final rejection as set forth in paper No.4 is withdrawn in response to applicants' amendments.
2. A new 103(a) rejection is made as set forth in this Office Action.
3. Applicant's cancellation to claim 17 is acknowledged.
4. Claim 18 is newly added.
5. Thus, claims 1-16 and 18 are pending in this application.

Drawings

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: reference character "15" is not disclosed on Fig.1a. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 12, 16 and 18 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In reference to claims 16 and 18, claim

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"...a low dielectric constant sheath surrounding each wire, said sheath covering substantially only said wire and wire connection to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads...". However, such limitation is not mentioned in the specification.

Furthermore, according to Fig.4A the low dielectric constant sheath (45) is covering a portion of the chip. Also, in reference to claim 12, applicants claim a device including an "open cavity". However, this "open cavity is not mentioned in the specification.

Appropriate correction is required.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1, 12, 16 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "substantially" in claims 1, 12, 16 and 18 render the claims indefinite since it fail to define the claimed invention.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 1, 3, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (U.S. 6,013,109) in view of Casto (U.S. 5,172,214).

In reference to claim 1, Choi (Figs.3A-3D) teaches a crack-resistance semiconductor package including a plurality of wire bonds (24) connecting pads on an integrated circuit chip (23) to conductive leads (25) of a semiconductor package; a low dielectric constant sheath (26) surrounding each wire (24); and a mold compound (29) encasing the chip (23), sheathed wires, and leads (25) (column 2, line 66 – column 3, line 45).

However, Choi fails to teach a plurality of parallel closely spaced wire bonds. However, Casto (Figs.1-2) in a related art to form a leadless package teaches a plurality of parallel closely spaced wire bonds (column 1, line 39 – column 4, line 21). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to include parallel closely spaced wire bonds as taught by Casto in the crack-resistance semiconductor package of Choi, since this reduce the size of the semiconductor package (column 2, lines 46 – 48).

In reference to claims 3, 10 and 11, Choi teaches that the thickness of the dielectric sheath is 2.5 microns minimum in each surface (column 3, lines 25-27); that the device is packaged in a ball grid array package; and that the device is packaged as a leaded surface mount package (column 2, line 66 – column 3, line 45).

13. Claims 2, 4-9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi ('109) in view of Casto ('214) as applied to claims 1, 3, 10 and 11 above, and further in view of Eysermans (U.S. 4,048,670).

In reference to claims 2, 8, 9 and 13, Choi in combination with Casto substantially teach all aspects of the invention but fails to show that the dielectric sheath

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comprises a foamed thermoplastic polymer consisting of polyurethane. However, Eysermans in a related art to stress-free package teaches using foamed polyurethane as a resilient material (column 4, lines 13-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use foamed polyurethane as taught by Eysermans to surround the bonding wires of the package device of Choi and Casto, since polyurethane is a material that can withstand shock (i.e. resilient), and can provide physical support against differential forces (column 4, lines 13-39).

In reference to claim 4, Choi in combination with Casto and Eysermans teach using foamed polyurethane as a dielectric sheath, but fails to expressly teach that the dielectric constant of the sheath surrounding bond wires is in the range of 1.0 to 2.3. However, since the material used as the dielectric sheath is the same as that of the claimed invention, it is inherently known that the dielectric constant of the sheath is in the range of 1.0 to 2.3.

In reference to claims 5, 6 and 7, Choi in combination with Casto and Eysermans substantially teach all aspects of the invention but fails to show that the distance between wires is in the range of 50 to 100 microns; the mutual capacitance between bond wires is lower by a factor of 3; and the dielectric constant of the molding compound is in the range of 3.8 to 4.2. However, the selection of the claimed ranges is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious)

and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

14. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi ('109) in view of Casto ('214) as applied to claims 1, 3, 10 and 11 above, and further in view of Featherby et al. (U.S 6,368,899).

Choi in combination with Casto substantially teach all aspects of the invention but fail to teach that the cavity package shell comprises a ceramic or a composite polymer. However, Featherby et al. (Fig.8) teach a package device in which a cavity package shell comprises a ceramic material (column 1, lines 8-35) or a composite polymer (12/300/400) (column 11, line 50 – column 12, line 29). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a ceramic cavity package shell as taught by Featherby et al. in the package device of Choi and Casto, since ceramic cavity packages are well-known materials used to prevent impurities from entering critical portions of the package (column 1, lines 23-27). It would also have been obvious to one of ordinary skill in the art to form a composite polymer cavity package shell as taught by Featherby et al. in the package device of Choi and Casto, since this would result in a hermetic package (column 3, lines 12-14).

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi ('109) in view of Kim et al. (U.S. 5,801,074).

Choi (Figs.3A-3D) teaches a crack-resistance semiconductor package including a substrate (21); a plurality of wire bonds (24) connecting pads on an integrated circuit chip (23) to conductive leads (25) of a semiconductor package; a low dielectric constant

sheath (26) surrounding each wire (24); and a mold compound (29) encasing the chip (23), sheathed wires, and leads (25) (column 2, line 66 – column 3, line 45).

Choi fails to teach a housing shell surrounding a cavity. However, Kim et al. (Figs.7a-7b) teach an air-tight semiconductor package including a housing shell (71) surrounding a cavity (column 3, line 24 – column 9, line 46). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the semiconductor package of Kim et al. in the crack-resistance semiconductor package of Choi et al., since this would result in a semiconductor package with improved air leakage and high yield (column 9, lines 18 – 46).

16. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi ('109) in view of Kim et al. Kobayashi et al. (U.S. 4,821,148).

Choi (Figs.3A-3D) teaches a crack-resistance semiconductor package including a substrate (21); a plurality of wire bonds (24) connecting pads on an integrated circuit chip (23) to conductive leads (25) of a semiconductor package; a low dielectric constant sheath (26) surrounding each wire (24); and a mold compound (29) encasing the chip (23), sheathed wires, and leads (25) (column 2, line 66 – column 3, line 45).

Choi fails to teach a sheath covering only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and no covering other portions of said chip and said conductive leads. However, Kobayashi et al. (Figs.1A-1C) teach a resin package semiconductor device including a sheath (7) covering only a wire (3) and wire connections to pads (4, 5) located on an integrated circuit chip (1) and on conductive leads (2), and no covering other portions of said chip (!) and said

conductive leads (2) (column 3, line 47 – column 6, line 17). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the sheath as taught by Kobayashi et al. in the crack-resistance semiconductor package of Choi, since this would provide protection against corrosive agents to the package (column 3, line 47 – column 6, line 17).

17. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi ('109) in view of Eysermans ('670) Kim et al. and Kobayashi et al. ('148).

Choi (Figs.3A-3D) teaches a crack-resistance semiconductor package including a substrate (21); a plurality of wire bonds (24) connecting pads on an integrated circuit chip (23) to conductive leads (25) of a semiconductor package; a low dielectric constant sheath (26) surrounding each wire (24); and a mold compound (29) encasing the chip (23), sheathed wires, and leads (25) (column 2, line 66 – column 3, line 45).

Choi fails to show that the dielectric sheath comprises a foamed thermoplastic polymer. However, Eysermans in a related art to stress-free package teaches using foamed polyurethane as a resilient material (column 4, lines 13-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use foamed polyurethane as taught by Eysermans to surround the bonding wires of the package device of Choi, since polyurethane is a material that can withstand shock (i.e. resilient), and can provide physical support against differential forces (column 4, lines 13-39).

Still, Choi in combination with Eysermans fail to teach a sheath covering only said wire and wire connections to said pads on said integrated circuit chip and to said

conductive leads, and no covering other portions of said chip and said conductive leads. However, Kobayashi et al. (Figs. 1A-1C) teach a resin package semiconductor device including a sheath (7) covering only a wire (3) and wire connections to pads (4, 5) located on an integrated circuit chip (1) and on conductive leads (2), and no covering other portions of said chip (!) and said conductive leads (2) (column 3, line 47 – column 6, line 17). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the sheath as taught by Kobayashi et al. in the semiconductor package of Choi and Eysermans, since this would provide protection against corrosive agents to the package (column 3, line 47 – column 6, line 17).

Conclusion

18. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

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Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.


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2823